AMENDMENTS TO THE CLAIMS

1. (Previously presented) A semiconductor device package (10, 100) comprising:

a molding compound (18) forming a portion of:

a first package face (14),

a second package face (12) opposite the first package face (14), and

package side faces (16) extending between the first and second package faces (14, 12);

a semiconductor device (20) at least partially covered by the molding compound (18), the semiconductor device (20) including a plurality of I/O pads (38); and

an electrically conductive lead frame (22) comprising:

a plurality of posts (24) disposed at a perimeter of the package (10, 100), each post (24) having a first contact surface (26) disposed at the first package face (14) and a second contact surface (28) disposed at the second package face (12) and having an edge surface extended entirely from the first package face to the second package face, the semiconductor device (20) being positioned in a central region defined by the plurality of posts (24), and

a plurality of post extensions (32), each post extension (32) having a third contact surface (34) disposed at the second package face (12), the plurality of post extensions (32) extending from the plurality of posts (24) toward the semiconductor device (20), each of the post extensions (32) including a bond site (36) formed on a surface of the post extension (32) opposite the second package face (12), at least one of the I/O pads (38) being electrically connected to the post extension (32) at the bond site (36),

wherein

the molding compound (18) is coplanar with side surfaces (60) of the posts (24) at the package side faces (16), and

two package side faces (16) meet to form a square corner at each of four corner regions of the package (10, 100).

2. (Original) The semiconductor device package (10) of claim 1, wherein the at least one of the I/O pads (38) is wire bonded or tape bonded to the bond site (36).

3. (Original) The semiconductor device package (10) of claim 2, wherein the die (20) is attached to a support pad (30), the support pad (30) including a surface extending along the second package face (12).

4. (Cancelled)

5. (Original) The semiconductor device package (10, 100) of claim 1, wherein the semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among two of the four package side faces (16).

6. (Original) The semiconductor device package (10, 100) of claim 1, wherein the semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among all of the four package side faces (16).

7-18. (Cancelled)

19. (New) The semiconductor device package (100) of claim 1, wherein the at least one of the I/O pads (38) is directly electrically connected to the bond site (36) for forming a flip-chip type connection.

20. (New) A stack of semiconductor device packages (10, 100), each semiconductor device package (10, 100) comprising:

a molding compound (18) forming a portion of:

a first package face (14),

a second package face (12) opposite the first package face (14), and

package side faces (16) extending between the first and second package faces (14, 12);

a semiconductor device (20) at least partially covered by the molding compound (18), the semiconductor device (20) including a plurality of I/O pads (38);

an electrically conductive lead frame (22) comprising:

a plurality of posts (24) disposed at a perimeter of the package (10, 100), each post (24) having a first contact surface (26) disposed at the first package face (14) and a second contact surface (28) disposed at the second package face (12) and having an edge surface extended entirely from the first package face to the second package face, the semiconductor device (20) being positioned in a central region defined by the plurality of posts (24), and

a plurality of post extensions (32), each post extension (32) having a third contact surface (34) disposed at the second package face (12), the plurality of post extensions (32) extending from the plurality of posts (24) toward the semiconductor device (20), each of the post extensions (32) including a bond site (36) formed on a surface of the post extension (32) opposite the second package face (12), at least one of the I/O pads (38) being electrically connected to the post extension (32) at the bond site (36);

wherein the first contact surfaces (26) of at least one of the semiconductor packages (10, 100) is directly electrically connected to one of the first and second contact surfaces (26, 28) of an adjacent semiconductor package (10, 100).

21. (New) The stack of semiconductor device packages (10) of claim 20, wherein the at least one of the I/O pads (38) is wire bonded or tape bonded to the bond site (36).

22. (New) The stack of semiconductor device packages (10) of claim 21, wherein the semiconductor device (20) is attached to a support pad (30), the support pad (30) including a surface extending along the second package face (12).

23. (New) The stack of semiconductor device packages (100) of claim 20, wherein the at least one of the I/O pads (38) is directly electrically connected to the bond site (36) for forming a flip-chip type connection.

24. (New) The stack of semiconductor device packages (10, 100) of claim 20, wherein each semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among two of the four package side faces (16).

25. (New) The stack of semiconductor device packages (10, 100) of claim 20, wherein each semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among all of the four package side faces (16).